Amendments to the Drawings

Please replace originally submitted sheet 6 of 10 with the Replacement Sheet for Sheet 6 of 10 submitted herewith. An Annotated Sheet Showing Changes for Sheet 6 of 10 is also submitted. The proposed corrected drawing sheet corrects errors in originally submitted FIG. 7 that would cause the depicted circuit to function improperly. Specifically, the polarity of several transistors and power supplies was inadvertently reversed in the originally submitted drawing. These polarity errors make the originally depicted circuit 144 of FIG. 7 function improperly. As depicted in originally submitted FIG. 5, circuit 144 is intended to implement the logic equations indicated on FIG. 5. The polarity errors in originally submitted FIG. 7 were inconsistent with the depiction of circuit 144 in FIG. 5. Specifically, the power supply values of three nodes were inverted from Vcc to Ground or vice versa and a total of nine transistors were converted from PMOS transistors to NMOS transistors or vice versa. It would be apparent to one skilled in digital logic that the circuit depicted in originally submitted FIG. 7 did not comply with the circuit or equations depicted in FIG. 5 and that the proposed corrected FIG. 7 does comply with the circuit and equations depicted in FIG. 5. Accordingly, Applicant submits that this amendment merely corrects an error that would be apparent to a skilled artisan and that this amendment does not introduce new matter.

Attachments:

1 Replacement Sheet for Sheet 6 of 10
1 Annotated Sheet Showing Changes for Sheet 6 of 10

REMARKS/ARGUMENTS

Claims 1-20 were presented and examined. The Examiner objected to informalities in the specification, drawings, and claims. The Examiner rejected claims 1-20 under 35 USC § 102(a), as being anticipated by Hayakawa (U.S. Patent Application No. 2001/0037349A1), hereinafter "Hayakawa". In this response, Applicant has amended claims 2, 3, 8, 12, 13, 15 18, canceled claims 1, 4-7, 10, 11, 14, 17 and added claims 21-25. Claims 2, 3, 8, 9, 12, 13, 15, 16, and 18-25 remain pending.

Specification Objections

The Examiner objected to informalities in the specification as filed. In response, Applicant has amended the abstract of the disclosure to comply with the 150 word limit.

Drawing Objections

The Examiner objected to informalities in the drawings as filed and required correction. In response to the objection to the claim 1 element reciting "a select circuit configured to select between a first sum and a second sum responsive to the carry-out bit", Applicant respectfully traverses the objection. Referring to FIG. 3, select circuits 136 are depicted to select between a first sum (the sum generated by circuits 132 and a second sum (the sum generated by circuits 134) responsive to a carry out bit (e.g., C_{16}, C_{32}, and C_{48}) in FIG. 3. Applicant believes that the claims only recite that which is shown in the drawings and Applicant would request the Examiner to reconsider and withdraw the objection or clarify the nature of the objection.

In response to the objection based on elements recited in claims 5 and 6, Applicant has canceled the claims causing the objection. Accordingly, Applicant would request the Examiner to withdraw the objection.

Applicant has submitted a proposed replacement sheet for originally submitted sheet 6 of 10 to correct some errors in the originally submitted sheet. A description of the proposed changes is described above under the heading "Amendment to the Drawings."

Claim Objections

The Examiner objected to informalities in claims 10 and 20. In response, Applicant has amended each of the objected-to claims.

Claim rejections under 35 USC § 102(a)

The Examiner rejected claims 1-20 under Section 102(a) as being anticipated by Hayakawa. In response, Applicant has canceled the independent claims 1 and 11 and re-written claims 3 and 13 in independent form incorporating the limitations of originally presented claims 1 and 11. Applicant respectively traverses the anticipation rejection of claims 3 and 13.

Anticipation is appropriate only when a single reference teaches all of the claim limitations either explicitly or inherently. MPEP 2131. Claims 3 and 13 recite limitations that are not taught either explicitly or inherently in the cited reference. Specifically, claims 3 and 13 are not anticipated by Hayakawa because Hayakawa does not disclose, either explicitly or inherently, the use of CMOS transmission gates.

The claimed CMOS transmission gate refer consistently throughout the specification to a PMOS and NMOS transistor combination in which a first source/drain terminal of the PMOS transistor is connected to a first source/drain terminal of the NMOS transistor and a second source/drain terminal of the PMOS transistor is connected to a second source/drain terminal of the NMOS transistor. See, e.g., the description of transmission gates 173, 174, and 175 in the paragraph beginning on page 10, line 24 and the corresponding illustration in FIG. 7. Those skilled in the art having the benefit of this disclosure will recognize that the claimed transmission gate circuits scale better than conventional pass logic (in which the input signals are applied to the transistor gates) and that the speed of the claimed transmission gate circuits is relatively independent of the gate voltage.

It is readily apparent from inspection of FIG. 21 of Hayakawa that the reference does not teach either explicitly or inherently a CMOS transmission gate as recited in the claims under discussion. There is no instance in Hayakawa in which the source/drain terminals of the PMOS transistor are connected to the source/drain terminals of an NMOS transistor as shown in FIG. 6 and FIG. 7 of the present invention. Hayakawa uses conventional MOS logic in which input signals are provided to the gate electrodes of NMOS transistors. A single PMOS transistor is

used in Hayakawa to pull up an output node to VCC when a clock signal is low (see, e.g., Node ND41 in FIG. 21(a) of Hayakawa). The source/drain terminals of the transistors in Hayakawa are connected in the traditional fashion (i.e., to either ground, VCC, or an intermediate node between ground and VCC. No input signal is applied to the source/drain terminals of the transistors in Hayakawa as is the case in the CMOS transmission gates of the present invention.

Applicant has expanded on details of the CMOS transistor gate technology or architecture of the presentation application in newly added claims 21-25. In claim 21, Applicant recites the design of a CMOS transmission gate explicitly. Claim 22 includes a limitation reciting that the transistor gate electrodes in the transmission gates are driven by complementary copies of a common signal. Claim 23 recites the details of the propagate circuit in which two CMOS transmission gates are used to provide an EXOR function. Claim 24 recites the group circuits of the present invention as including a set of transmission gates arranged in series. Finally, claim 25 recites a group circuit wherein each transmission gate is controlled by one of the propagate bits. Because all of these limitations are fully supported by FIG. 6 and FIG. 7 and the accompanying text, the new claims add no new matter. Each of the newly added claims recites explicitly distinctions between the transmission gates as that term is used in the specification and conventional MOS logic of Hayakawa. Because the reference does not disclose limitations found in claims 3 and 13 or in newly added claims 21-25, Applicant would respectfully request the Examiner to reconsider and withdraw the rejection of claims 3 and 13 and all claims depending thereon.

CONCLUSION

In this response, Applicant has addressed the Examiner's objections to the specification, drawings, and claims, and claim rejections under 35 USC § 102(a). Accordingly, Applicant believes that this response constitutes a complete response to each of the issues raised in the office action. In light of the amendments made herein and the accompanying remarks, Applicant believes that the pending claims are in condition for allowance. Accordingly, Applicant would request the Examiner to withdraw the rejections, allow the pending claims, and advance the application to issue. If the Examiner has any questions, comments, or suggestions, the undersigned attorney would welcome and encourage a telephone conference at 512.428.9872.

Respectfully submitted,

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